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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/006,551	11/30/2001	Christopher D.S. Donham	NVIDP064/P000286	2643

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EXAMINER	
AMIN, JWALANT B	

ART UNIT	PAPER NUMBER
2628	

NOTIFICATION DATE	DELIVERY MODE
12/22/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/006,551	DONHAM ET AL.	
	Examiner	Art Unit	
	JWALANT AMIN	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114 was filed in this application after a decision by the Board of Patent Appeals and Interferences, but before the filing of a Notice of Appeal to the Court of Appeals for the Federal Circuit or the commencement of a civil action. Since this application is eligible for continued examination under 37 CFR 1.114 and the fee set forth in 37 CFR 1.17(e) has been timely paid, the appeal has been withdrawn pursuant to 37 CFR 1.114 and prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 11/16/2009 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claims 1-30 have been considered but are moot in view of the new ground(s) of rejection.

3. Regarding claims 1-30, the applicant argues that none of the cited references teach "... an instruction set is received in response to the instruction request, the instruction set including a plurality of instructions such that the plurality of instructions are received at a single time for performing at least one optimization operation, the at least one optimization operation including at least one of combining at least a portion of the plurality of instructions, modifying at least a portion of the plurality of instructions, and deleting at least a portion of the plurality of instructions" (see pg. 9-10).

4. However, the examiner interprets that Rivard and Wang, and in view of Ando and further in view of Ireton teaches the above limitations. Please refer to the rejections below for further details.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-12, 18-21, 24-28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rivard (US 5,987,567), in view of Wang (5,831,640), in view of Ando (US 5497496) and further in view of Ireton (US 5826089).

7. Regarding claims 1, 21, 24-27 and 30, Rivard (Fig. 6, Fig. 10, col. 4 lines 46-57, col. 6 lines 45-67, col. 7 lines 1-10) teaches a method for execution with a system including a tangible computer readable medium, the method for retrieving instructions from video memory (DRAM 655) utilizing a texture module (texture mapping stage 645 and texel cache system 650 combined together corresponds to texture module) in a graphics pipeline (graphics pipeline 640), comprising

sending an instruction request to video memory, where a texture module in a graphics pipeline sends the instruction request to the video memory (a texture mapping stage sends information to texel cache system; the texture mapping stage and the texel cache system together are considered as texture module, so the information is passed

between the components of the texture module; texel cache system comprising the memory request generator, pipeline latency elements, and cache data store and memory data resolver forwards the memory requests/read requests to DRAM for information retrieval (the examiner interprets that memory requests/read requests for all misses that are forwarded to DRAM are instruction requests based on which DRAM sends back information; the examiner relies on the definition of instruction provided by dictionary.com, which defines instructions as a command given to a computer to carry out a particular operation and can contain data to be used in the operation; here DRAM sends memory data based on the memory requests/read requests from the texture module. Memory requests/read requests act as an instruction to DRAM, which performs a particular function based on the request); and

receiving instructions from the video memory in response to the instruction request utilizing the texture module in the graphics pipeline (DRAM returns memory data to cache data store and memory data resolver component of texel cache system, which further sends this information to the texture mapping stage; the texture mapping stage and the texel cache system together are considered as texture module, so the information/memory data is passed between the components of the texture module).

Although Rivard discloses the limitations as stated above, Rivard does not explicitly teach to combine texture mapping stage and texel cache system to form a texture module. However, it would have been obvious to one of ordinary skill in art at the time of present invention to combine texture mapping stage and texel cache system of Rivard to work together as a texture module. The unity of diversity of parts would

depend more upon the choice of the manufacturer, and the convenience and availability of the machines and tools necessary to construct the texture module, than on any inventive concept. One of ordinary skill in art, furthermore, would have expected applicant's invention to perform equally well with Rivard's reference that teaches to send and receive information/instruction from the texture mapping stage and texel cache system to the DRAM because using this components together will also result in sending and receiving instructions to and from DRAM. Therefore, it would have been obvious to one of ordinary skill in art at the time of present invention to modify Rivard to obtain the invention as specified in the claim.

Rivard also teaches the arrival of memory data and associated instructions at the cache data store and memory data resolver component of the text cache system is coordinated by pipeline latency elements (col. 7 lines 4-7; memory data has associated instructions). Although Rivard discloses the limitations as stated above, Rivard does not explicitly teach that the memory returns instructions along with data, in response to instruction request from the texture module. However, Wang teaches a graphics subunit (texture module) in a graphics hardware system that supplies data and control signals to local frame buffer memory for executing a series of display instructions (Fig. 1, col. 5 lines 38-67; the computer memory includes the local frame buffer memory, which corresponds to the DRAM; based on the control signals send by the graphics hardware system, the frame buffer returns the polygon display instructions that includes the texture data, so that the graphics subunit executes the display instructions using this data). Therefore, it would have been obvious to one of ordinary skill in art at the time of

present invention to have the memory return instructions as taught by Wang to the texture module of Rivard because these instructions are needed to render the graphics primitives to be displayed on the display device (col. 5 lines 43-45 and lines 63-67).

Although the combination of Rivard and Wang teach the limitations as stated, they do not explicitly teach an instruction set is received in response to the instruction request (fig. 4 shows that instruction fetch circuit 2 sends an instruction request to the instruction memory 1 and receives a plurality of instructions), the instruction set including a plurality of instructions such that the plurality of instructions are received at a single time. However, Ando teaches exactly the same (fig. 4, col. 1 lines 39-55, col. 2 lines 1-48; it should be noted that a plurality of instructions are fetched from the instruction memory in the same cycle). Therefore, it would have been obvious to one of ordinary skill in the art at the time of present invention to fetch a plurality of instructions in the same cycle as taught by Ando and apply it into the method of Rivard and Wang because such a method can enhance the performance by processing instructions in parallel (col. 1lines 27-36).

Although the combination of Rivard, Wang and Ando teach the limitations as stated, they do not explicitly teach the plurality of instruction performs at least one optimization operation (combining portions of multiple source instructions), the at least one optimization operation including at least one of combining at least a portion of the plurality of instructions, modifying at least a portion of the plurality of instructions, and deleting at least a portion of the plurality of instructions. However, Ireton teaches exactly the same (Abstract, col. 2 lines 51-59). Therefore, it would have been obvious to one of

ordinary skill in the art at the time of present invention to combine multiple source instructions as taught by Ireton and apply it into the method of Rivard, Wang and Ando because the execution core is more efficiently utilized by combining portions of multiple source instructions into a target instructions, which increases performance of the microprocessor (col. 2 lines 42-59).

8. Regarding claim 2, Rivard teaches a method and system for retrieving instructions from memory utilizing a texture module in a graphics pipeline, comprising sending a texture request (texture lookup requests) to memory utilizing the texture module in the graphics pipeline (Fig. 6, col. 6 lines 50-60).

9. Regarding claim 3, Rivard teaches receiving texture information (memory data) from the memory in response to the texture request utilizing the texture module in the graphics pipeline (Fig. 6, col. 6 lines 50-56).

10. Regarding claim 4, Rivard teaches the video memory includes a frame buffer (col. 3 lines 5-10).

11. Regarding claim 5, Rivard teaches the memory includes direct random access memory (DRAM) (col.4 lines 32-35 and lines 45-55).

12. Regarding claim 6, Rivard teaches the instructions are adapted for controlling a texture environment module (pipeline latency elements) coupled to the texture module (Fig.6, Fig.10).

13. Regarding claim 7, Rivard teaches the instructions control the manner in which the texture environment module processes the texture information (col.7 lines 3-7).

14. Regarding claim 8, Rivard teaches receiving initial instructions from a rasterizer module (graphic accelerator having graphic pipeline stage shows that the texture module receives data/instructions from the upper modules of the pipeline) coupled to the texture module (Fig.6).

15. Regarding claim 9, Rivard teaches the initial instructions control at least the sending of the instruction request by the texture module (Fig. 6; graphic accelerator having graphic pipeline stage shows that the texture module receives data/instructions from the upper modules of the pipeline; thus based on these instructions, the texture module sends the instruction request to the DRAM).

16. Regarding claim 10, Rivard teaches temporarily storing the instructions and the texture information in cache (cache data store and memory data resolver) (Fig. 6, Fig. 10).

17. Regarding claim 11, Rivard teaches the cache is resident on the texture module (Fig.6, Fig.10).

18. Regarding claim 12, Rivard teaches that each piece of texture information and each of the instructions are of a similar size in the memory (col. 6 lines 50-67 and col. 7 lines 1-15; texture mapping stage includes the ALU which reformats data including resizing of texel data types for uniformity).

19. Regarding claim 18, although Rivard teaches the above-discussed limitations, Rivard does not explicitly teach a complete instruction set is received in response to the instruction request. However, Wang (col. 5 lines 43-67, col. 6 lines 1-47) teaches a graphics subunit (texture module) of a graphics hardware system executing a series of

display instructions (set of instructions) stored in computer memory. The graphics subunit receives display instructions including texture data based on the supplied data and control signals (the single display instruction received by the graphics from the sub-routine process in response to the control signals correspond to a complete set of instruction; this instruction in the sub-routine is executed by the graphics subunit for rendering the concerned graphics primitive, and therefore it is considered as a complete set of instruction). Therefore, it would have been obvious to one of ordinary skill in art at the time of present invention to have the memory return a complete set of instructions as taught by Wang to the texture module of Rivard because this instruction set is needed to render the concerned graphics primitive (col. 5 lines 43-45 and lines 63-67).

20. Regarding claims 19, although Rivard teaches the above-discussed limitations, Rivard does not explicitly teach a partial instruction set is received in response to the instruction request. However, Wang (col. 5 lines 43-67, col. 6 lines 1-47) teaches a graphics subunit (texture module) of a graphics hardware system executing a series of display instructions (set of instructions) stored in computer memory. The graphics subunit receives display instructions including texture data based on the supplied data and control signals (the single display instruction received by the graphics from the sub-routine process in response to the control signals correspond to a partial set of instruction; this instruction in the sub-routine is executed by the graphics subunit for rendering the concerned graphics primitive, but other instructions are needed for rendering other primitives, and therefore overall this single instruction is considered as a partial set of instruction). Therefore, it would have been obvious to one of ordinary skill

in art at the time of present invention to have the memory return instructions as taught by Wang to the texture module of Rivard because these instructions are needed to render the graphics primitives to be displayed on the display device (col. 5 lines 43-45 and lines 63-67).

21. Regarding claim 20, the statements presented above, with respect to claims 1 and 19, are incorporated herein.

22. Regarding claim 28, Rivard teaches a texture mapping stage as shown in Fig. 6 receiving data (instructions) from the rasterizer module of the pipeline and then receiving data (instructions) from the DRAM. Thus the instructions received from the DRAM via the texel cache system are considered to be the additional instructions. Please refer to the rejection of claims 1, 2, 3, 8 and 10 for further details regarding the rejection of other limitations.

23. Claims 13-17, 22, 23, 29, are rejected under 35 U. S.C. 103(a) as being unpatentable over Rivard, Wang, Ando and Ireton, and further in view of Applicant Admitted Prior Art (AAPA).

24. Regarding claim 13, although the combination of Rivard, Wang, Ando and Ireton teach a method and system for retrieving instructions from memory utilizing a texture module in a graphics pipeline, they do not explicitly teach controlling the texture module utilizing a shader module coupled thereto. However, AAPA teaches controlling the texture module utilizing a shader module coupled thereto (Fig.3; shader module is also coupled to the rasterizer module). Therefore, it would have been obvious to a person of

ordinary skill in the art at the time of the invention to incorporate the shading module of AAPA into the texture module of Rivard, Wang, Ando and Ireton because combination of shading module and texture module would enable a shading function to the graphic pipeline.

25. Regarding claim 14, although the combination of Rivard, Wang, Ando and Ireton teach a method and system for retrieving instructions from memory utilizing a texture module in a graphics pipeline, they do not explicitly teach the shader module controls the sending of instruction request and texture request by the texture module. However, AAPA teaches this limitation (Fig. 3 page 5 lines 24-31).

26. Regarding claim 15, although the combination of Rivard, Wang, Ando and Ireton teach a method and system for retrieving instructions from memory utilizing a texture module in a graphics pipeline, they do not explicitly teach the shader module processes a plurality of pixels with the texture information based on the instructions. However, AAPA teaches this limitation (Fig. 3).

27. Regarding claim 16, although the combination of Rivard, Wang, Ando and Ireton teach a method and system for retrieving instructions from memory utilizing a texture module in a graphics pipeline, they do not explicitly teach the shader module is capable of reusing the texture information in order to request further texture information from the video memory (control the looping of texture process). However, AAPA teaches this limitation (Fig. 3 page 4 lines 24-31).

28. Regarding claim 17, although the combination of Rivard, Wang, Ando and Ireton teach a method and system for retrieving instructions from memory utilizing a texture

module in a graphics pipeline, they do not explicitly teach ceasing the processing upon the receipt of terminate instruction (require significant amount of time to push down the pipeline). However, AAPA teaches this limitation (Fig. 3 page 5 lines 7-15).

29. Regarding claims 22, 23, although the combination of Rivard, Wang, Ando and Ireton teach a method and system for retrieving instructions from memory utilizing a texture module in a graphics pipeline, they do not explicitly teach the texture module is adapted for operating in a plurality of different modes. However, AAPA teach texture module is adapted for operating in a plurality of different modes. See page 3 lines 20-25. It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate texture module of Rivard from the system of Rivard, Wang, Ando and Ireton into the texture module of AAPA because a combination of texture module operating in plurality of difference modes and the texture module of Rivard would provide components of the texture module processing the texels in various ways such as an address calculation module allow various dimensionality textures.

30. Regarding claim 29, the statements presented above, with respect to claims 1, 2, 3, 8, 10, 13, 14, 15, 17 and 28 are included herein.

Conclusion

31. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Vassiliadis et al. (US 5051940)
- Savkar et al. (WO 96/38783)

- Hayakawa et al. (EP 862112)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JWALANT AMIN whose telephone number is (571)272-2455. The examiner can normally be reached on 10:30 a.m. - 7:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on 571-272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kee M Tung/
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